page 3 line 26 TEH 10/24/03

(2) Please replace the sentence at page 4, line 13 with the following: Still another commonly assigned, related application, U.S. Serial No. 09/528753, filed on March 20, 2000, teaches the use of silicides in vertical MOSFETs.

a2 NE

IN THE CLAIMS

a3

10. (Amended) The structure of claim 1 wherein the doped regions are configured to form an inverter circuit.

REMARKS

Claims 1-31 remain in the application. Claims 2-31 have been withdrawn as subject to a restriction requirement which the undersigned has traversed. Claims 1-13 and 15-19 are rejected while claim 14 is objected to as dependent from a rejected claim.

In the most recent office action the examiner has inquired about the publication date of the Hergenrother reference. After conferring with Mr. Hergenrother as well as referring to information made available by the IEEE, it was concluded that the publication date of the subject reference is December 1999. Specifically, the paper was presented during the meeting held beginning on December 5 and ending on December 8 of 1999.

The drawings have been objected to. Formal drawings are submitted with this filing. A copy is attached to this paper for the examiner's convenience. The specification has been amended per the examiner' request. A new abstract is attached to this paper.

All of the rejections under section 103 are based on Fitch in combination with Woo. Applicants respectfully request that the examiner reconsider this rejection as an

improper one. That is, any combination of Fitch and Woo would require a hindsight reconstruction of Fitch in order to meet the terms of applicants' claims. Specifically, with regard to independent claim 1, Fitch fails to disclose, "a conductive layer formed between the first and second regions and above the plane..."

With the dielectric layer 16 of Fitch formed, by all appearances, directly upon the layer 40 in which the diffusions 44 and 46 are formed (Figure 9) the Fitch reference would have to be piecemeal modified in order to create the claimed invention. No such modification is taught or suggested by any of the art of record.

A similar deficiency persists with regard to the rejection of claim 15. Specifically, with applicant's claimed structures of a "first source/drain region formed in the first layer, a channel region formed over the first layer and a second source/drain region formed over the channel region..." a reconstruction of the Figure 9 Fitch embodiment is required in order to configure a "conductive layer...between the first source/drain region of each transistor to conduct current from one first source/drain region to the other first source/drain region." None of the art of record alone or in combination teaches or suggests any such combination.

It is further noted that each of the dependent claims further distinguishes the invention.

For all of the above reasons, removal of the rejection is in order and it is respectfully submitted that the application is now in condition for allowance.

Attached hereto is a marked-up version of the changes made to the specification, claims and abstract by the current amendment. The attached page is captioned "Version With Markings to Show Changes Made."

Respectfully,

By _____
Ferdinand M. Romano
Reg. No. 32,752
407-371-3250

Date: 10 July 2002

Version With Markings to Show Changes Made

(1) Kindly write page 4, line 7 as follows: CMOS integrated circuits having PMOS transistors integrated with NMOS transistors are well known, and a process for fabricating CMOS vertical MOSFETs is described in U.S. Serial No. 09/335646 [290533] entitled, "A CMOS Integrated Circuit Having Vertical Transistors and a Process of Fabricating Same, " filed on June 18, 1999, now incorporated by reference.

(2) Kindly write page 4, line 13 as follows: Still another commonly assigned, related application, U.S. Serial No. 09/528753, [341,190] filed on March 20, 2000, teaches the use of silicides in vertical MOSFETs.

(3) Kindly write claim 10 as follows: The structure of claim 1 wherein the doped [diffusion] regions are configured to form an inverter circuit.

(4) Kindly write the abstract as follows: [An architecture for connection between regions in or adjacent a semiconductor layer. Generally, an integrated circuit structure, having a semiconductor layer with a major surface formed along a plane, includes first and second spaced-apart doped regions formed in the surface. A third doped region of different conductivity type than the first region is positioned over the first region. A conductive layer comprising a metal is formed between the first and second regions and above the surface plane, providing electrical connection between the doped regions.]

An architecture for connection between regions in or adjacent a semiconductor layer. According to one embodiment of the invention a

semiconductor device includes a first layer of semiconductor material and a first field effect transistor having a first source/drain region formed in the first layer. A channel region of the transistor is formed over the first layer and an associated second source/drain region is formed over the channel region. The device includes a second field effect transistor also having a first source/drain region formed in the first layer. A channel region of the second transistor is formed over the first layer and an associated second source/drain region is formed over the channel region. A conductive layer comprising a metal is positioned between the first source/drain region of each transistor to conduct current from one first source/drain region to the other first source/drain region.

In one embodiment of an associated method of manufacture a first device region, selected from the group consisting of a source region and a drain region of a field effect transistor, is formed on a semiconductor layer. A second device region, selected from the group consisting of a source region and a drain region of a field effect transistor, is also formed on the semiconductor layer. A conductor layer comprising metal is positioned adjacent the first and second device regions to effect electrical connection between the first and second device regions. A first field effect transistor gate region is formed over the first device region and the conductor layer and a second field effect transistor gate region is formed over the second device region and the conductor layer.

[In another associated method for fabricating a semiconductor device a first device region, selected from the group consisting of a source region and a drain region of a field effect transistor, is formed on a semiconductor layer and a

second device region, selected from the group consisting of a source region and a drain region of a field effect transistor is also formed on the semiconductor layer. A conductor layer is positioned adjacent the first and second device regions to effect electrical connection between the first and second device regions. A first field effect transistor gate region is formed over the first device regions and the conductor layer and a second field effect transistor gate region is formed over the second device region and the conductor layer.]

ABSTRACT

An architecture for connection between regions in or adjacent a semiconductor layer. According to one embodiment of the invention a semiconductor device includes a first layer of semiconductor material and a first field effect transistor having a first source/drain region formed in the first layer. A channel region of the transistor is formed over the first layer and an associated second source/drain region is formed over the channel region. The device includes a second field effect transistor also having a first source/drain region formed in the first layer. A channel region of the second transistor is formed over the first layer and an associated second source/drain region is formed over the channel region. A conductive layer comprising a metal is positioned between the first source/drain region of each transistor to conduct current from one first source/drain region to the other first source/drain region.

In one embodiment of an associated method of manufacture a first device region, selected from the group consisting of a source region and a drain region of a field effect transistor, is formed on a semiconductor layer. A second device region, selected from the group consisting of a source region and a drain region of a field effect transistor, is also formed on the semiconductor layer. A conductor layer comprising metal is positioned adjacent the first and second device regions to effect electrical connection between the first and second device regions. A first field effect transistor gate region is formed over the first device region and the conductor layer and a second field effect transistor gate region is formed over the second device region and the conductor layer.